## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A frequency multiplier comprising:

a phase shift section generating at least one phase shift signal [[for]] based on a fundamental signal;

a waveform combining section generating a combined waveform by combining signal waveforms of the same polarity obtained by wave-rectifying the fundamental signal and the phase shift signal; and

a comparator section comparing the combined waveform with a variable comparison threshold voltage based on a frequency of a multiplied waveform.

2. (Original) The frequency multiplier according to claim 1, further comprising a level shift section for shifting amplitude levels of at least any one of the fundamental signal and the phase shift signal prior to the generation of the combined waveform.

3. (Original) The frequency multiplier according to claim 1, wherein the phase shift section comprises a phase inverting section.

4. (Original) The frequency multiplier according to claim 3, wherein the phase inverting section comprises a differential pair.

5. (Original) The frequency multiplier according to claim 1, wherein the phase shift section comprises at least one of a phase advancing section and a phase delaying

section for generating the phase shift signal having a prescribed phase difference with respect to the fundamental signal.

6. (Original) The frequency multiplier according to claim 5, wherein the at least one of the phase advancing section and the phase delaying section comprises one of a capacitive load element and an inductive load element.

7. (Previously Presented) The frequency multiplier according to claim 1, wherein the comparator section can adjust the comparison threshold voltage as appropriate.

8. (Original) The frequency multiplier according to claim 2, wherein the level shift section can adjust the amplitude levels as appropriate for each of the fundamental signal and the phase shift signal.

9. (Original) The frequency multiplier according to claim 2, wherein the level shift section comprises a switching control section for switching, as appropriate, driving ability for each of the fundamental signal and the phase shift signal.

10. (Original) The frequency multiplier according to claim 9, wherein the driving ability is a size of a transistor for outputting the fundamental signal or the phase shift signal.

11. (Original) The frequency multiplier according to claim 9, wherein the driving ability is a current value of a driving current source for outputting the fundamental signal or the phase shift signal.

12. (Original) The frequency multiplier according to claim 9, wherein the driving ability is a size of a load element for determining a voltage level of the fundamental signal or the phase shift signal.

13. (Canceled).

14. (Previously Presented) The frequency multiplier according to claim 1, wherein the waveform combining section comprises a full-wave rectifier section.

15. (Previously Presented) The frequency multiplier according to claim 1, further comprising:

an input differential pair for receiving the fundamental signal at at least one of differential input terminals thereof, and for outputting differential output signals;

a first level shift section for biasing the differential input terminals by proper DC voltages, respectively;

a full-wave rectifier section for full-wave-rectifying the differential output signals; and

a first comparator section for comparing a full-wave-rectified signal that is output from the full-wave rectifier section with a reference voltage as the comparison threshold voltage.

16. (Currently Amended) The frequency multiplier according to claim 1, further comprising:

an input differential pair for receiving the fundamental signal at [[at]] least one of differential input terminals thereof, and for outputting differential output signals from differential output terminals thereof;

high-pass filter sections provided for the respective differential output terminals, for interrupting DC components that are output from the respective differential output terminals;

a second level shift section for biasing differential signals that are output from the high-pass filter sections by proper DC voltages, respectively;

a full-wave rectifier section for full-wave-rectifying output signals of the second level shift section; and

a second comparator section for comparing a full-wave-rectified signal that is output from the full-wave rectifier section with a reference voltage as the comparison threshold voltage.

17. (Original) The frequency multiplier according to claim 16, further comprising a differential amplifier section between the second level shift section and the full-wave-rectifier section, wherein the output signals of the second level shift section

are input to the full-wave rectifier section after being amplified by the differential amplifier section.

18. (Original) The frequency multiplier according to claim 15, further comprising:

two or more input differential pairs for receiving the fundamental signal and the at least one phase shift signal having the prescribed phase difference with respect to the fundamental signal; and

one of a phase advancing section and a phase delaying section for generating each phase shift signal individually.

19. (Original) The frequency multiplier according to claim 15, wherein the first level shift section further comprises a switching control section for switching, as appropriate, sizes of transistors of a transistor pair of the input differential pair or resistance values of load resistors of the input differential pair.

20. (Original) The frequency multiplier according to claim 15, wherein load resistors that are connected to the input differential pair are active loads including MOS transistors, and the first level shift section further comprises a switching control section for switching and controlling bias voltages for gate terminals of the respective MOS transistors.

21. (Original) The frequency multiplier according to claim 15, wherein load resistors that are connected to the input differential pair are active loads including bipolar transistors, and the first level shift section comprises a switching control section for switching and controlling base currents flowing through base terminals of the respective bipolar transistors.

22. (Original) The frequency multiplier according to claim 18, wherein the first level shift section comprises a switching control section for switching and controlling current values of bias current sources for driving the input differential pairs.

23. (Original) The frequency multiplier according to claim 1, further comprising an FM modulator, wherein the fundamental signal is obtained by frequency-modulating an original signal with the FM modulator when the original signal is a frequency signal.

24. (Original) The frequency multiplier according to claim 1, further comprising a V/F converter, wherein the fundamental signal is a frequency signal obtained by converting an original signal with the V/F converter when the original signal is a voltage signal.